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Term	Documents
(12 AND 14).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	19
(L12 AND L14).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	19

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<u>L15</u>	L12 and l14	19	<u>L15</u>
<u>L14</u>	L13 same cache	350	<u>L14</u>
<u>L13</u>	(status or state or dirty) same (RAM or random access memory) same (table or directory or structure or list)	7345	<u>L13</u>
<u>L12</u>	(snoop or snooping) same cache same dirty	292	<u>L12</u>
<u>L11</u>	(status or state or dirty) same (RAM or random access memory)	48826	<u>L11</u>
<u>L10</u>	L9 and (14 or 15)	14	<u>L10</u>
<u>L9</u>	cache same (flush or flushing) same (write adj back) same l3	15	<u>L9</u>
<u>L8</u>	L7 and (15 or 14)	105	<u>L8</u>
<u>L7</u>	cache same (flush or flushing) same (write adj back)	272	<u>L7</u>
<u>L6</u>	cache same (flush or flushing) same (write adj back) same l3 same (14 or 15)	8	<u>L6</u>
<u>L5</u>	("L3" or (level adj three) or (third adj level)) adj2 cache	496	<u>L5</u>
<u>L4</u>	("L2" or (level adj two) or (second adj level)) adj2 cache	3482	<u>L4</u>
<u>L3</u>	("L1" or (level adj one) or (first adj level)) adj2 cache	2329	<u>L3</u>
<u>L2</u>	operating system same l1	9	<u>L2</u>
<u>L1</u>	(variable or programmable) same cache same (way or set) same (associativity or associative)	114	<u>L1</u>

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- | | | |
|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
| 1
 | Cache coherence in systems with parallel communication channels & many processors
John C. Willis , Arthur C. Sanderson , Charles R. Hill
Proceedings of the 1990 ACM/IEEE conference on Supercomputing
November 1990
This paper describes and analyzes two algorithms for maintaining cache coherence in multiprocessor systems with parallel communication channels and many processors. A distributed link-list relates all cache frames representing the same main memory block. Messages traverse the list to maintain list integrity, exclusive ownership, and consistent values. Memory access semantics are equivalent to a shared memory system without caches. Reference latency, efficiency of memory use, and hardware complex ... | 98% |
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 | The software lookaside buffler reduces search overhead with linked lists
Gerald Bozman
Communications of the ACM March 1984
Volume 27 Issue 3 | 96% |